Remarks

In the present response, seven claims (1, 8, 10, 17, 19, 24, 31) are amended. Claims 1-36 are presented for examination.

I. Claim Objections

Claims 8, 17, and 27 are objected to because they are allegedly duplicative of claims 7, 16, 24. This rejection is moot since claims 8, 17, and 27 are amended.

II. Double Patenting

Claims 1, 10, and 31 are rejected on the ground of non-statutory obviousness-type double patenting. This rejection is moot since a terminal disclaimer is enclosed with this response.

III. Claim Rejections: 35 USC § 102(b)

Claims 1-36 are rejected under 35 USC § 102(b) as being anticipated by USPN 5,812,811 (Dubey). Applicants respectfully traverse this rejection.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since Dubey neither teaches nor suggests each element in the claims, these claims are allowable over Dubey.

The independent claims recite numerous recitations that are not taught or even suggested in Dubey. By way of example, claim 1 recites a pre-execution thread that runs "ahead of the main thread in program order to cause data to be cached before the main thread needs the data." Nowhere does Dubey teach or even suggest that a thread runs ahead of the main thread so data is cached before the main thread needs the data. Dubey teaches future threads that "can be executed concurrently with the forking thread which continues to execute the sequence of instructions sequentially following the FORK" (see Dubey at 8: 60-65). Dubey, however, never discloses that the future threads run ahead of the forking thread to cause data to be cached before the forking thread needs the data.

For at least these reasons, independent claim 1 and its dependent claims are allowable over Dubey.

Independent claims 10, 19, and 31 recite numerous recitations that are not taught or even suggested in Dubey. By way of example, each of these independent claims recites the following or a variation thereof: "so cache misses encountered by the second thread are resolved before the first thread encounters the cache misses." Nowhere does Dubey teach or even suggest that a second thread runs ahead of the main thread so cache misses encountered by the second thread are resolved before the main thread encounters the cache misses. Dubey teaches future threads that "can be executed concurrently with the forking thread which continues to execute the sequence of instructions sequentially following the FORK" (see Dubey at 8: 60-65). Dubey, however, never discloses that the future threads run ahead of the forking thread so cache misses encountered by the future thread are resolved before the forking thread encounters the cache misses.

For at least these reasons, independent claim 10, 19, and 31 and their dependent claims are allowable over Dubey.

CONCLUSION

In view of the above, Applicants believe that all pending claims are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. 832-236-5529. In addition, all correspondence should continue to be directed to the following address:

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

/Philip S. Lyren #40,709/

Philip S. Lyren
Reg. No. 40,709
Ph: 832-236-5529